REMARKS

Claims 60-62, 64, 69, 71-76, and 89-92 were pending in the present application. By virtue of this response, Claims 71-72 are cancelled and Claim 64 amended. Accordingly, Claims 60-64, 69, 73-76 and 89-92 are currently under consideration. Amendment and cancellation of claims is not to be construed as a dedication to the public of any of the subject matter of the claims as previously presented.

Claim Rejections - 35 USC § 103(a)

Claims 60-62, 64, 69, 71-76, and 89-92 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Hogan (U.S. 5,699,434) in view of Tanaka (U.S. 4,885,750).

The Examiner stated in pertinent part:

> Hogan fails to explicitly disclose that the DSV data patterns are incorporated immediately following at least two headers in the control data of the application file to ensure the DSV data patterns are accesses and wherein information about the size of each header in the control data is modified to include the DSV data patterns.
>
> However, Tanaka et al. teaches placing DSV data patterns in such locations (see column 2 lines 43-54 where information about the size of the header must incorporate the included DSV data patterns to prevent errors).

Further, the Examiner rejected dependent Claims 71 and 72 citing Hogan column 6 lines 40-50, Figure 4, and column 6 lines 42-67.

Rejections are Traversed

Applicant respectively traverses the rejections.

The paragraph of Tanaka cited by the Examiner at column 2 lines 43-53 says:

> One block of the data including the paraties is divided into 59 frames FRM0 through FRM58, each of which is added with a header including a sync signal SYNC having a predetermined bit pattern, an identification signal representing contents of the program, a pre-emphasis constant etc., and a digital sum value control bit DSC for reducing a dc component and low-frequency components in the transmitted digital signals, as shown in FIGS. 6 and 7. And the data including the paraties are transmitted frame by frame in synchronism with every fourth horizontal sync pulse of the video signal.

This paragraph references Tanaka et al. FIG. 6 and 7. The most relevant figure is FIG. 7 showing the blocks. As shown there is the sync section which is 11 bits long, the ID section which is 4 bits long, the DSV section which is 1 bit long, followed by 61 bytes of data. This single DSV bit is the "digital sum value control bit DSC for reducing a dc component and low-frequency components in the transmitted digital signals" at column 2 lines 48-50 and quoted above. As can be seen, this is a single bit. It is also characterized as a "bit" at column 2 line 49. Moreover the purpose of this bit is clearly stated in the above passage "for reducing a dc component and low-frequency components in the transmitted digital signals" (emphasis added).

So first this is only a single bit per header. That is, the header for the entire block includes only the single digital sum value control bit DSC. Moreover the purpose of this bit DSC is clearly stated as reducing the dc component and low-frequency components. As set forth in the present specification, these components are the cause of DSV problems. In other words, the purpose of this bit is to reduce DSV type problems. It is not explained how this occurs, but clearly the purpose is reduction of DSV problems resulting from a dc component and low-frequency components.

Hence there is only a single bit in Tanaka, not a bit "pattern". Moreover the purpose of Tanaka's bit is to reduce DSV problems. So this bit DSC is neither a data pattern (it is only a single bit) and moreover its purpose is to prevent DSV problems. Note that there is no description in Tanaka of deliberately introducing DSV problems; apparently these are merely naturally occurring DSV problems.

Therefore the rejection of Claim 64 as previously pending is traversed. First, Claim 64 at line 4 recites "incorporating into the application file DSV data patterns". While admittedly Hogan has DSV data patterns, it is clear that Tanaka does not. Tanaka only has the single bit DSC. Moreover the whole purpose of bit DSC Tanaka is to reduce DSV problems. So Tanaka teaches away from both in Hogan and the present invention. Hence it is not seen why one would take the DSC bit from Tanaka and combine it with Hogan since they have opposite purposes, Hogan to cause DSV problems and Tanaka to reduce them. Moreover Hogan is dealing with actual data patterns. Instead Tanaka only has the single bit. Hence it is not seen why taking the single bit in the header of Tanaka and combining with the teachings of Hogan would result in the present invention. Presumably this combination would result in a single DSV bit being present in the header. Of course the single DSV bit would have no negative DSV effect as in Hogan, but would have the positive (reduction) effect as indicated by Tanaka. Hence Tanaka and Hogan teach opposites. It is not seen how or why they would be combined to meet the present invention. So the rejection of Claim 64 is traversed.

Claim Amendments

In order to even more clearly distinguish over Tanaka and Hogan, Claim 64 has been amended. First, Claim 64 is amended to include the subject matter of Claims 71 and 72 (now canceled) to specify the nature of the DSV data patterns. This makes it clear that these are indeed patterns and they have particular recited result which is "the DSV has a significant absolute value or the DSV data patterns are repeated patterns of values." It is understood that the Examiner found this subject matter in Hogan. However it is not present in Tanaka and moreover Tanaka only has the single bit related to DSV. This makes it clear that Tanaka does not teach data patterns of the type in Hogan or in accordance with the present invention.

Further the final clause of Claim 64 as amended now recites "wherein for each header information about the size of the header in the control data is modified to include at least one of the DSV data patterns." This reads on the present specification paragraph 92.

Again this feature is not shown or suggested in Hogan or Tanaka. In Hogan the DSV data patterns are not in the headers. Even if the Examiner considers the single bit in Tanaka to be somehow relevant to causing DSV problems, it is not in fact a DSV data pattern, but is only a single bit. The single bit does not meet and cannot accomplish the feature now recited in Claim 64 as amended relating to the DSV data patterns which are "to ensure that the DSV has a significant absolute value or the DSV data patterns are repeated patterns of values." Clearly in Tanaka bit DSC accomplishes neither, and further in Tanaka the bit DSC is only a single bit per header and so by definition could not have a significant absolute DSV value or be a repeated pattern of values.

Hence even the combination of Tanaka and Hogan (which combination in fact does not make any sense or have any justification as pointed out above) fails to meet Claim 64 both as previously pending and as amended and therefore Claim 64 is allowable thereover.

The remaining dependent claims are all dependent upon Claim 64 and allowable for at least the same reason as the base claim.

CONCLUSION

In view of the above, all pending claims in this application are believed to be in immediate condition for allowance, and the Examiner is respectfully requested to withdraw the outstanding rejections of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark Office determines that an extension and/or other relief is required, Applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Attorney Docket No. 136922004600.

Rule 34

This paper is filed under Rule 34; the correspondence address remains that of Patent Department, Macrovision Corporation.

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